| TITLE | DOC No. RFD-20240808013-001 | |
|---|---|---|
| 400G QSFP-DD SR4 Transceiver | REVISION : 01 | AUTHORIZED BY : Andy Yang |
| | DATE : 2026.02.06 | CLASSIFICATION : Optics Transceiver |

## 1. General Description

This product is a 400Gb/s QSFP-DD400 400G SR4 optical module designed for 100m optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, The module converts four 100Gb/s parallel optical signals into eight (PAM4) electrical output data, each running at 50Gb/s, for a total data rate of 400Gb/s.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP- DD400 400G SR4 module receptacle. Host FEC is required to support up to 100m fiber transmission.

## 2. PRODUCT FEATURES

- Compliant to QSFP-DD/QSFP-DD800/QSFP112 HWRev 6.2
- Compliant with CMIS 4.0
- Parallel 4 Optical Lanes
- IEEE 802.3db 400GBASE-SR4 Specification compliant
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Up to 100m transmission with OM4 MMF
- Maximum power consumption 9W
- MPO-12 Receptacle
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃

RoHS 2.0 complain

## 3. PRODUCT DESCRIPTION

### 3.1 PRODUCT NAME

**400G QSFP-DD SR4**

| Data Rate | Wavelength (nm) | Distance | Fiber Type | Power (dBm) | Sen. (dBm) | Connector | Tem. |
|---|---|---|---|---|---|---|---|
| 400G SR4 | 850 | 100m | MMF | -4.6~4 | -4.6 | MPO-12 | C |

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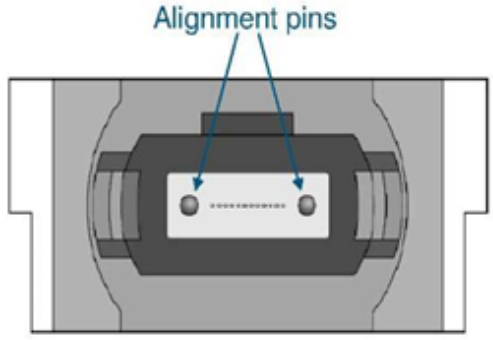
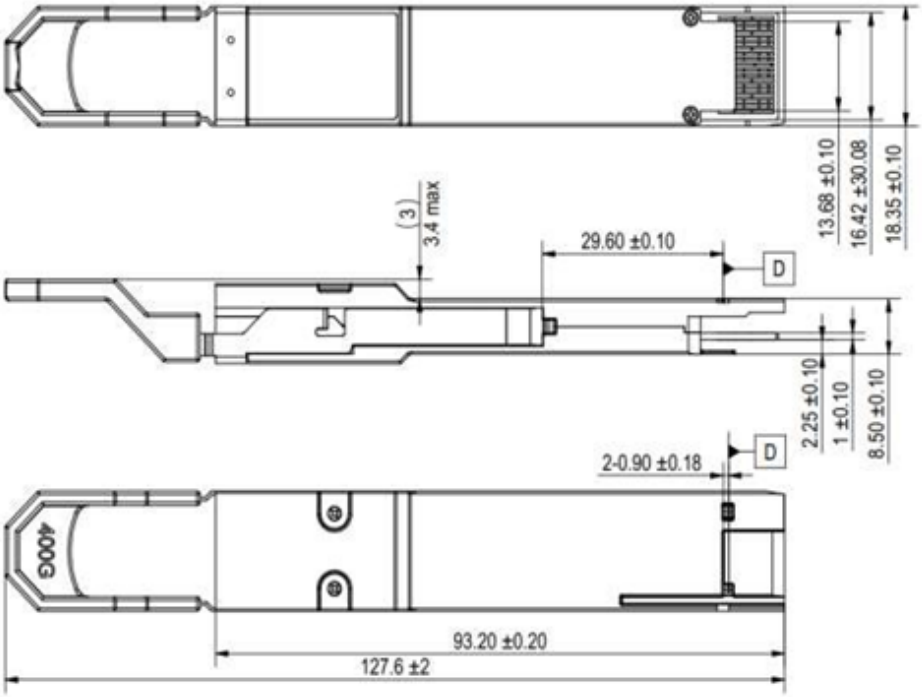
### 3.2 DIMENSIONS,MATERIALS,PLATINGS AND MARKING




Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1




Unit : mm

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## 4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

## 5. Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Storage Temperature Range | $T_{STG}$ | -40 | +85 | °C |
| Supply Voltage | $V_{CC}$ | 0.5 | 3.6 | V |
| Relative Humidity | RH | 10% to 90% non-condensing | | |

## 7. Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Case Temperature- Operating | $T_{CASE}$ | 0 | 70 | °C |
| Supply Voltage | Vcc | 3.135 | 3.465 | V |
| Power Consumption | $P_{DISS}$ | | 9 | W |
| Pre-FEC Bit Error Ratio | | | $2.4x10^{-4}$ | |
| Link Distance over OM3 | | 0.5 | 60 | M |
| Link Distance over OM4 | | 0.5 | 100 | M |

## 8. Transmitter Optical Specifications

| Transmitter Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|
| Signaling rate each lane | 53.125±100ppm | | | GBd |
| Lane Wavelength Range | | 850 | | nm |

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| | | | | |
|---|---|---|---|---|
| RMS Spectral width | | | 0.6 | nm |
| Modulation Format | PAM4 | | | |
| Average Optical Power per lane | -4.6 | | 4 | dBm |
| Outer Optical Modulation Amplitude (OMAouter), each lane<br>for TDECQ<=1.8dB<br>for 1.8<TDECQ<=4.4dB | <br><br>-2.6<br>-4.4+TDECQ | | <br><br>3.5<br>3.5 | dBm |
| Outer Optical Modulation Amplitude (OMAouter), each lane<br>for TECQ<=1.8dB<br>for 1.8<TECQ<=4.4dB | <br><br>-2.6<br>-4.4+TECQ | | <br><br>3.5<br>3.5 | dBm |
| Transmitter and Dispersion Eye Closure for PAM4, each Lane | | | 4.4 | dB |
| Transmitter Eye Closure for PAM4(TECQ), each Lane | | | 4.4 | dB |
| Extinction Ratio | 2.5 | | | dB |
| Tranmitter excursion ,each lane | | | 2 | dB |
| Trasmitter transition time,each lane | | | 17 | ps |
| Average Launch Power per Lane @ TX Off State | | | -30 | dBm |
| Relative Intensity Noise12(OMA) | | | -131 | dB/Hz |
| Optical Return Loss Tolerance | | | 12 | dB |
| Encircled Flux | >=86% at 19um<br><=30% at 4.5um | | | dB |

## 9. Receiver Optical Specifications

| Receiver Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|
| Signaling rate each lane | 53.125±100ppm | | | GBd |
| Lane Wavelength Range | | 850 | | nm |
| Modulation Format | PAM4 | | | |
| Damage Threshold | 5 | | | dBm |

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| | | | | |
|---|---|---|---|---|
| Average Receive Power, each lane | -6.4 | | 4 | dBm |
| Receiver Power, each lane (OMA) | | | 3.5 | dBm |
| Receiver Sensitivity each lane ($OMA_{outer}$)<br>for TECQ<=1.8dB<br>for 1.8<TECQ<=4.4dB | | | -4.6<br>-6.4+TECQ | dBm |
| Receiver reflectance | | | -12 | dB |
| Stressed Receiver Sensitivity ($OMA_{outer}$), each | | | -2 | dBm |
| Stressed Conditions for Stress Receiver Sensitivity | | | | |
| Stressed Eye Closure for PAM4 (SECQ),Lane under Test | | 4.4 | | dB |
| OMAouter of each Aggressor Lane | | 3.5 | | dBm |

## 10. Receiver Thresholds for Loss of Signal (LOS)

| Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|
| RX_LOS_Assert Min/Max | -15.0 | | | dBm |
| RX_LOS_De-Assert Min/Max | | | -8.9 | dBm |
| RX_LOS_Hysteresis | | 1.5 | | dB |

## 11. Digital Diagnostic Monitoring Specifications

| Parameters | Unit | Specification |
|---|---|---|
| Temperature Monitor absolute error | ° C | ± 3 |
| Supply Voltage Monitor absolute error | % | ± 5 |
| I_bias Monitor absolute error | % | ± 10 |
| Received Power (Rx) Monitor absolute error | dB | ± 3.0 |
| Transmit Power (Tx) Monitor absolute error | dB | ± 3.0 |

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## 12. Low Speed Electrical signal

| Parameter | Symbol | Min | Max | Units | Condition |
|---|---|---|---|---|---|
| SCL and SDA | VOL | 0 | 0.4 | V | IOL(max)=3.0mA for fast mode,20mA for Fast-mode plus |
| | VOH | Vcc-0.5 | Vcc+0.3 | V | |
| SCL and SDA | VIL | -0.3 | Vcc*0.3 | V | |
| | VIH | Vcc*0.7 | Vcc +0.5 | V | |
| Capacitance for SCL and SDA I/O pin | Ci | | 14 | pF | |
| Total bus cpacitive load for SCL and SDA | Cb | | 100 | pF | 3.0k Ohms Pull up resistor,max |
| | | | 200 | pF | 1.6k Ohms Pull up resistor,max |
| LPMode/TxDis,Reset and ModeSelL | VIL | -0.3 | 0.8 | V | \|Iin\| </= 125uA for Vin < Vcc |
| | VIH | 2 | Vcc + 0.3 | V | |
| IntL/RxLOS | VOL | 0 | 0.4 | V | IOL=2.0mA |
| | VOH | VCC - 0.5 | VCC + 0.3 | V | 10k ohms pull-up to Host Vcc |
| ModPrsL | VOL | 0 | 0.4 | % | IOL=2.0mA |
| | VOH | | | | ModPrsL can be implemented as a short-circuit to GND on the module |

## 13. Low Speed Electrical signal

| Parameter | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|
| **Receiver electrical output characteristics at TP4** | | | | | |
| Signaling rate per lane | | 26.5625 | | GBd | |
| AC common-mode output voltage(RMS) | | - | 17.5 | mV | |

| TITLE | DOC No. RFD-20240808013-001 | |
|---|---|---|
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| | | | | | |
|---|---|---|---|---|---|
| Differential peak-to-peak output voltage | | | 900 | mV | |
| Near-end ESMW (Eye symmetry mask width) | | TBD | | UI | |
| Near-end Eye height, differential | 24 | | | mV | |
| Near-end vertical eye closure | | | 7.5 | dB | |
| Far-end ESMW (Eye symmetry mask width) | | TBD | | UI | |
| Far-end Eye height, differential | 24 | | | mV | |
| Far-end vertical eye closure | | | 7.5 | dB | |
| Far-end pre-cursor ISI ratio | | TBD | | % | |
| Common mode to differential conversion return loss | 802.3ck 120G-1 | | | dB | |
| Effective return loss | TBD | | | dB | |
| Differential termination mismatch | | | 10 | % | |
| Transition time (min, 20% to 80%) | | TBD | | ps | |
| DC common mode voltage | -350 | | 2850 | mV | |
| **Transmitter electrical input characteristics at TP1** | | | | | |
| Signaling rate, per lane | | 26.5625 | | GBd | |

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| | | | | | |
|---|---|---|---|---|---|
| Differential pk-pk input voltage tolerance | 900 | | | mV | |
| Common-mode to differential return loss | 802.3ck Equation(120G-1) | | | | |
| Effective return loss | TBD | | | | |
| Differential termination mismatch | | | 10 | % | |
| Module stressed input test | See 120G.3.4.1 | | | | |
| Single-ended voltage tolerance range | -0.4 | | 3.3 | V | |
| DC common-mode voltage | -350 | | 2850 | mV | |

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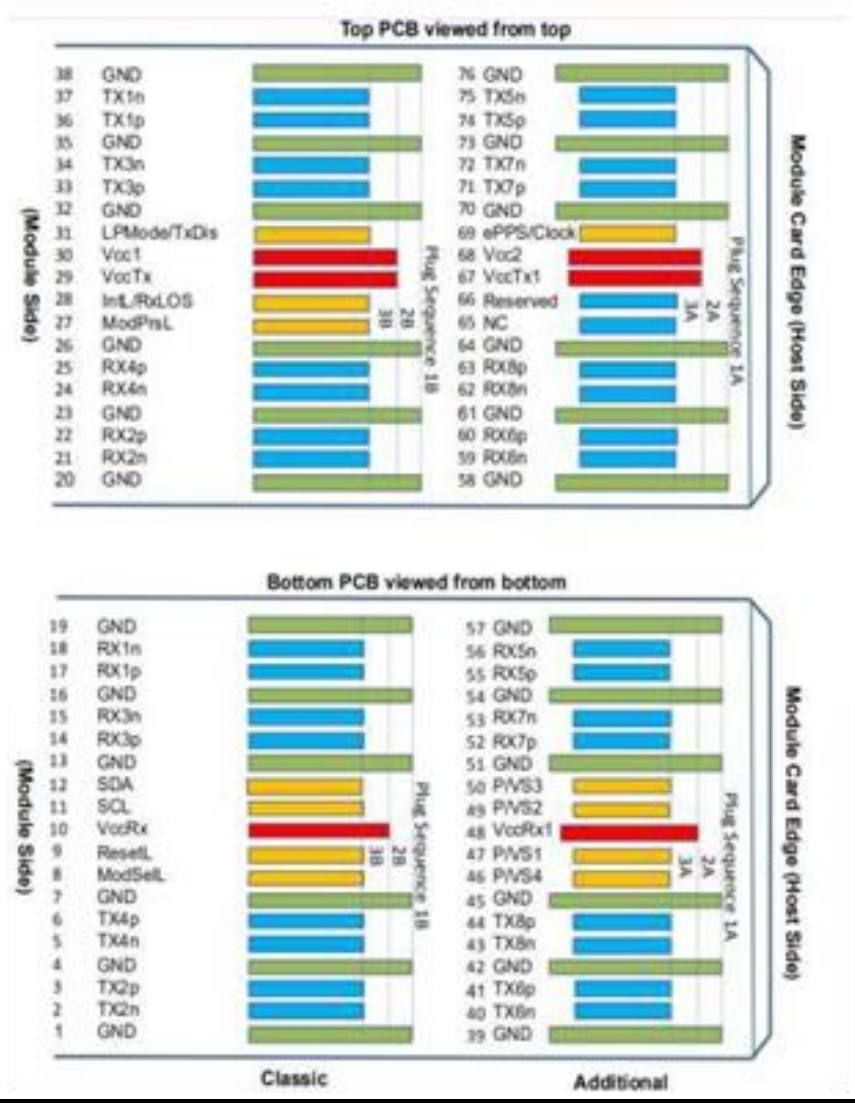
## 14. QSFP-DD400 400G SR4 Edge Connector and Pinout




### Module contact definition

| TITLE | DOC No. RFD-20240808013-001 | |
|---|---|---|
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**Pad Function Definition**

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1B | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B | |
| 4 | | GND | Ground | 1B | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B | |
| 7 | | GND | Ground | 1B | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3B | |
| 9 | LVTTL-I | ResetL | Module Reset | 3B | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B | 2 |
| 11 | LVCMOS-I/O | SCL | TWI serial interface clock | 3B | |
| 12 | LVCMOS-I/O | SDA | TWI serial interface data | 3B | |
| 13 | | GND | Ground | 1B | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B | |
| 16 | | GND | Ground | 1B | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B | |
| 19 | | GND | Ground | 1B | 1 |
| 20 | | GND | Ground | 1B | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B | |
| 23 | | GND | Ground | 1B | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B | |
| 26 | | GND | Ground | 1B | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B | |
| 28 | LVTTL-O | IntL/ RxLOS | Interrupt/optional RxLOS | 3B | |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2B | 2 |
| 31 | LVTTL-I | LPMode/ TxDis | Low Power mode/optional TX Disable | 3B | |
| 32 | | GND | Ground | 1B | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B | |
| 35 | | GND | Ground | 1B | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B | |
| 38 | | GND | Ground | 1B | 1 |
| 39 | | GND | Ground | 1A | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A | |
| 42 | | GND | Ground | 1A | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A | |
| 45 | | GND | Ground | 1A | 1 |

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| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 46 | LVCMOS /CML-I | P/VS4 | Programmable/Module Vendor Specific 4 | 3A | 5 |
| 47 | LVCMOS /CML-I | P/VS1 | Programmable/Module Vendor Specific 1 | 3A | 5 |
| 48 | | VccRx1 | 3.3V Power Supply | 2A | 2 |
| 49 | LVCMOS /CML-O | P/VS2 | Programmable/Module Vendor Specific 2 | 3A | 5 |
| 50 | LVCMOS /CML-O | P/VS3 | Programmable/Module Vendor Specific 3 | 3A | 5 |
| 51 | | GND | Ground | 1A | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A | |
| 54 | | GND | Ground | 1A | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A | |
| 57 | | GND | Ground | 1A | 1 |
| 58 | | GND | Ground | 1A | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A | |
| 61 | | GND | Ground | 1A | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A | |
| 64 | | GND | Ground | 1A | 1 |
| 65 | | NC | No Connect | 3A | 3 |
| 66 | | Reserved | For future use | 3A | 3 |
| 67 | | VccTx1 | 3.3V Power Supply | 2A | 2 |
| 68 | | Vcc2 | 3.3V Power Supply | 2A | 2 |
| 69 | LVCMOS-I | ePPS/Clock | 1PPS PTP clock or reference clock input | 3A | 6 |
| 70 | | GND | Ground | 1A | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A | |
| 73 | | GND | Ground | 1A | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A | |
| 76 | | GND | Ground | 1A | 1 |

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

Note 3: Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.

Note 6: ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

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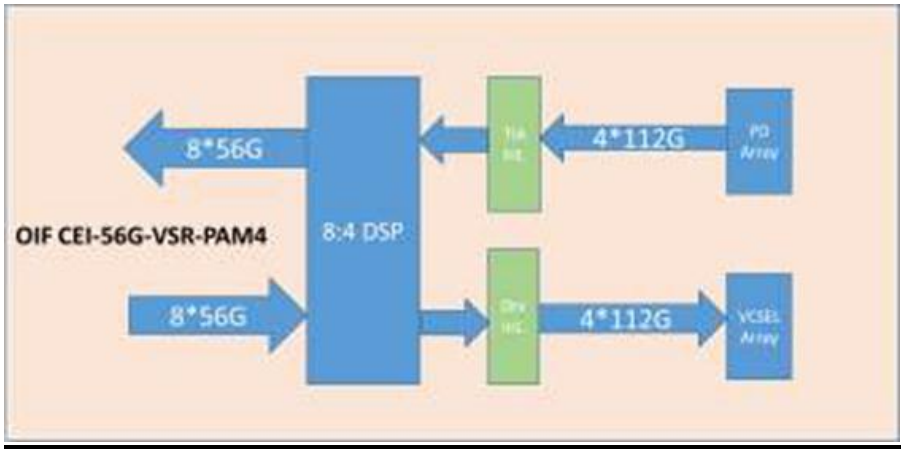
## Module Block Diagram




## 8.Modification History

| Rev. | Comments | Date | Originator | Approval |
|---|---|---|---|---|
| 01 | Preliminary Draft | 2026.02.06 | Andy Yang | Mike Sun |
| | | | | |